## G.H.RAISONI COLLEGE OF ENGINEERING AND MANAGEMENT, AMRAVATI

### Computer Science and Engineering Department

**SUBJECT: ADIC** **SEMESTER: IV** **SUBJECT CODE: 4KS02**

# QUESTION BANK

## UNIT I

1. Draw the Circuit of inverting amplifier and non inverting amplifier using op-amp and obtain the expression for voltage gain.
2. Define slew rate. What are the causes of slew rate?
3. An instantaneous input change of 10 V is applied to an op-amp connected as an unity gain amplifier. The output takes 20μs to change by 10V. What is the slew rate of op-amp?
4. Describe an active integrator circuit using op-amp with neat diagram. State its limitations.
5. Draw the circuits for Schmitt Trigger using op-amp and explain its operation waveforms.
6. Draw the circuit for summing amplifier using op-amp and explain its operation. Derive the expression for output voltage. How these circuits act as average circuits?
7. Draw and explain a simple op-amp differentiator, mention its limitations. Explain how it can be overcome in a practical differentiator.
8. Draw the circuit for differential amplifier using op-amp and derive the expression for output voltage.
9. An op-amp has a slew rate of 0.5V/μs. What is the largest sine wave output possible at a frequency of 1 MHz and what maximum output voltage of 1 v peak?

## UNIT II

1. Explain the working of a timer IC 555 as a monostable multivibrator with neat diagram and waveforms, Also derive expression for pulse width.
2. Draw transfer characteristics of PLL and explain.
3. Draw circuit using IC 555 for square wave generator and explain.
4. With neat diagram explain application of PLL as FM detector.
5. Explain the functions of the following pins of IC 555:
   a. Discharge
   b. Control Voltage
   c. Trigger
6. Draw circuit for a stable multivibrator using IC 555 and explain its operation.
7. Draw circuit for frequency translator using PLL and explain its working.

## UNIT III

1. Convert the decimal numbers 98.98 and 420.024 to Binary, Octal and Hexadecimal number system.
2. Convert the following decimal numbers to Binary, Octal and Hexadecimal number system: 1776, 1812, 1969, 2000.
3. Perform the following using 2's complement:
   a. 11011 – 10000
   b. 100 – 101000
   c. 10110 – 1011
   d. 1011100 – 1011100
4. Convert the decimal numbers 8.9 and 543.81 to Binary, Octal and Hexadecimal number system.
5. Convert the following decimal numbers to Binary, Octal and Hexadecimal number system: 654, 93948, 43, and 200.
6. Convert $(3794)_8$, $(6875)_8$ to Binary, Decimal and Hexadecimal number system.
7. Find Gray code and Excess 3 codes for $(01110)_2$, $(10110111)_2$.
8. Convert $(3FA7)_{16}$, $(8CE4)_{16}$ to Binary, Decimal and Octal number system.
9. Perform the following using 1's and 2's complement:

a. 101101 – 1001
b. 101010 – 111100

## UNIT IV

1. Reduce the following Boolean Expressions to required number of literals:
   a. BC+A'B'C+A'BC+ABC'+A'B'C' to five literals.
   b. BC+AC'+AB+BCD to four literals.
2. Simplify using K-map and implement using NOR gates:
   $F(A,B,C,D) = \sum m (0,2,5,7,13,15,18,20,21,23,28,29,31)$
3. Reduce (A+C+D) (A+C+D') (A+C'+D) (A+B') to four literals.
4. Simplify using K-map and implement using NAND/NOR gates.
   a. $F(W,X,Y,Z) = \prod M (0,1,2,5,8,9,10,13)$
   b. $F(W,X,Y,Z) = \sum m (0,2,5,7,8,10,11,14,15) + \sum d (3,12)$
   c. $F(A,B,C,D) = \sum m (0,2,5,7,13,15,18,20,21,23,28,29,31)$
   d. $F(W,X,Y,Z) = \prod M (0,1,2,5,8,9,10,13)$
5. Solve the following function using Tabular Method and K-map and realize the solution using NAND Gates:
   a. $F(A,B,C,D) = \sum m (1,3,5,10,11,12,13,14,15)$
   b. $F(A,B,C,D) = \sum m (0,2,5,7)$
   c. $F(A,B,C,D) = \sum m (1,3,5,10,11,12,13,14,15)$
   d. $F(A,B,C,D) = \sum m (0,2,5,7,8,10,11,14,15) + \sum d (1,13)$

## UNIT V

1. Design BCD to Excess 3 Code Convertor using Logic gates.
2. Explain Priority Encoder in brief.
3. Construct 3:8 line decoder.
4. Design BCD to Gray Code Convertor using Logic gates.
5. Design a combinational circuit that accepts a 2-bit number and generates a 4-bit binary number output equal to the square of the input number.
6. Design Half and Full Adder.
7. Design Half and Full Subtractor.
8. Design a combinational circuit that accepts a 3-bit number and generates output equals to 1 if the input variables have equal or more than 1's than 0's otherwise output is 0.

## UNIT VI

1. Construct Excitation Tables for SR FF, JK FF, D FF and T FF.
2. Design a 3-bit Synchronous Counter.
3. Design a synchronous counter to count the sequence 1-2-5-3-0-7 using T-FF.
4. Construct Truth Tables for SR FF, JK FF, D FF and T FF and find Characteristic equations for each.
5. Design a 3-bit Asynchronous Counter.
6. Design a synchronous counter to count the sequence 5-3-1-0-6 using T-FF.
7. Construct Truth Tables for SR FF, JK FF, D FF and T FF and also find Characteristic equations for each.
8. Design a 4 bit ripple carry adder.